Bus Design Parameters

- Bus Width
  # Address Lines – **n** lines can address $\mathbf{2^n}$ memory locations
  Physical space on motherboard, Connector size
  # Data Lines
  Bandwidth – Cycle Time (Bus Skew), Data Width
  Expansion and Backward *Compatibility*
  Multiplexing Address and Data

- Bus Clocking
  Synchronous – All bus operations are **clocked** and occur are predetermined times
  Asynchronous – Master/Slave coordination via **handshaking**

- Bus Arbitration
  Resolving simultaneous requests to control the bus
  Centralized – **daisy chaining**
  Decentralized

- Bus Operations
  Single Word Transfer
  Block Transfer
  Critical Section (Multiprocessor systems)
  Interrupt Requests

Synchronous Buses (1)

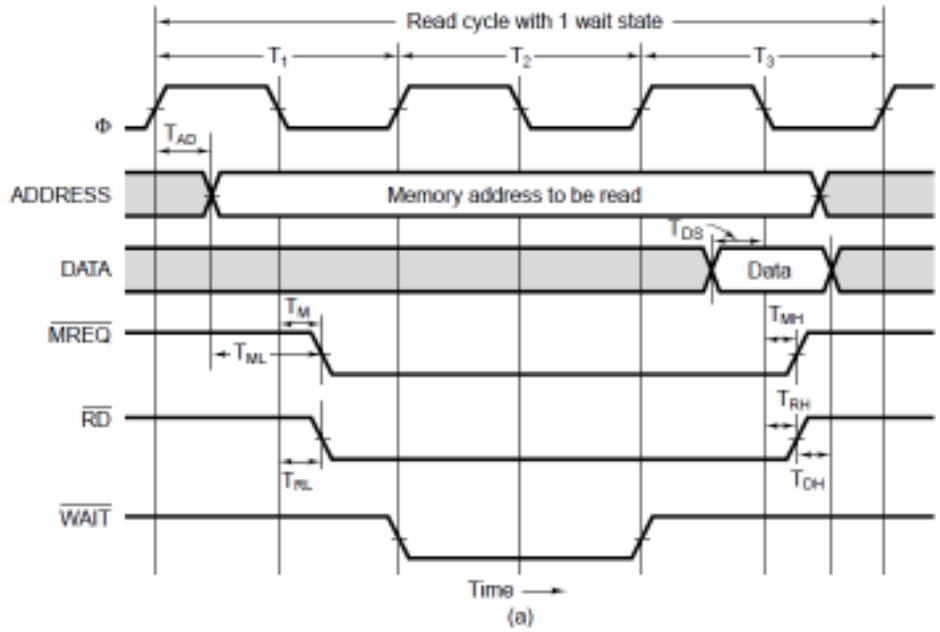

Figure 3-38. (a) Read timing on a synchronous bus.

CPU-Bus Memory Access

- CPU begins initiates memory read at the rising edge of a clock cycle T1 by latching address bits onto the bus. CPU asserts control signals MREQ & RD on the falling edge of cycle T1.
  1. Output a memory address onto the bus
     TAD: Address Output Delay - time for address lines to settle (Max 4 ns)
  2. Assert MREQ (Memory CS) and RD. Address bits must stabilize prior to MREQ.
     TML: time to wait before asserting control signals (Min 2 ns)
     TM: MREQ Output delay - time for MREQ line to settle (Max 3 ns)
     TRL: RD Output delay – time for RD line to settle (Max 3 ns)
- Bus inserts Wait State(s) to allow enough time for memory to place data onto DATA lines
  When WAIT is asserted, CPU cannot strobe data. Negated when data available.
- CPU begins strobing data off the bus at the falling edge of a clock cycle
  TDS: Time for data to settle before being strobed (Min 2 ns)
- CPU negates control signals after strobing data off the bus
  TMH: Time elapsed after date strobed until MREQ is negated (Max 3 ns)
  TRH: Time elapsed after date strobed until RD is negated (Max 3 ns)
  TDH: Time data must be held on the bus after RD negated (Min 0 ns)