Basics of Micro Architecture

ch3: Circuits

Logic gates → Multiplexer, Demultiplexer

Multiple input streams → 1 stream → 1 stream → multiple channels

Encoder, Decoder

Input devices — Output devices

Latch, Flip-flop

I/O devices — Fast storage

Adder — HA, FA ✓

Shifter — L shift, R shift

Bus — interface multiple units

Hierachy of virtual machines.

Level-2 ISA (opcode operand) — complex binary

Level-1: Microarchitecture level — Interpret Level-2 instructions

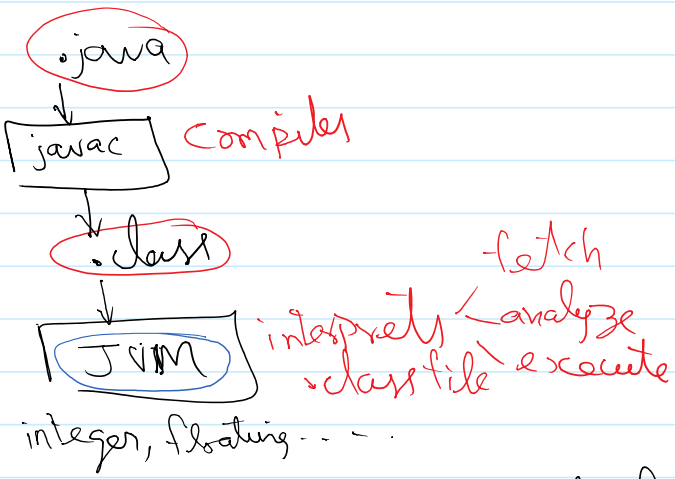
fetch ISA inst → analyze & decode → execute

Level-0 Digital Logic Level — minimize cost (primitive operation)

using

ISA

Java:



chosen TJVM (Integer Java Virtual Machine)

chosen IJVM (Integer Java Virtual Machine)
integer operands.

Level-2 IJVM (.class - Java bytecode)
↓ 24 Opcodes
Microarchitecture
Primitive DLL

IJVM
? What are opcodes & their semantics.

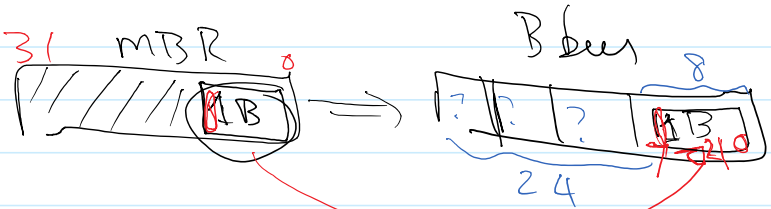
P262 20 opcodes
4 opcodes — IN, OUT, ERR, HALT } 24 opcodes

Mic Data Path (DLL - CPU HW)

Von Neumann:

4byte MAR
4byte MDR } to perform data read/write — L1-Data cache

4byte PC
MBR 1byte } to perform instruction fetch (ijvm) 1byte — L1-Instn cache



① MBRU: 24 bits to zeros (unsigned)
② MBR: 24 bits will be set as the 7th bit of MBR (signed / sign extended)

ALU operations (primitive)

Arithmetic: + ✓, −

*	−X
/	−Y
%	−X

$X - Y \Rightarrow X + (-Y)$

$\Rightarrow X + 2$'s compl (Y)

$\Rightarrow X +$ 1's compl $(Y) + 1$

$B + INV(A) + 1$

1 CPU cycle

Logical: AND, OR, NOT ✓

Shift

Need for INVA control signal (Subtraction operation in 1 CPU cycle)

6 ALU control signals: F_0, F_1, ENA, ENB, INVA, INC

Shifter

SLL8

SRA1

No shift

	SLL8	SRA1
No shift	0	0
SRA1	0	1
SLL8	1	0
Undefined	1	1

Control signals needed to drive the data path:

B bus:	4 (encoded)
C bus:	9 (separate)
ALU:	6
Shifter:	2
Memory R, W, F	3

24 signals = 0.4 ns

2.4 GHz

Microinstruction: A set of control signals
- that drives the data path.

Microprogram: A sequence of microinstructions.
has control flow: if condition branch MIX
MIY
allows to reuse microinstruction