

School of Computer Science

Course Title: Structured Computer Organization

Date: 11/5/03

Course Number: CDA-4101

Number of Credits: 3

Subject Area: Computer Systems	Subject Area Coordinator: Masoud Sadjadi email: sadjadi@cis.fiu.edu
Catalog Description: Covers the levels of organization in a computer: Design of memory, buses, ALU, CPU; design of microprogram. Covers virtual memory, I/O, multiple processes, CISC, RISC and parallel architectures.	
Textbook: Structured Computer Organization, 4 th Edition Andrew S. Tanenbaum Prentice Hall (ISBN: 0130959901)	
References: Computer Organization and Design: The Hardware/Software Interface, 2 nd Edition David A. Patterson, John L. Hennessy, Nitin Indurkha Morgan Kaufmann (ISBN: 1558604286)	
Prerequisites Courses: COP 3402, COP 3337 and MAD 2104	
Corequisites Courses: None	

Type: Required

Prerequisites Topics:

- Digital logic and boolean algebra
- Machine level representation of data
- Assembly level machine organization
- Fundamental data structures

Course Outcomes:

1. Master the design of memory, ALU, control unit, and design of microprogram
2. Be familiar with cache architectures, branch predictions and scheduling of multiple instruction issue
3. Be familiar with instruction set architecture, interrupts, and traps
4. Be familiar with CISC and RISC architectures, and parallel computer configurations
5. Be exposed to shared-memory and message-passing multicomputers, and cache coherence protocols

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Outline

Topic	Number of Lecture Hours	Outcome
<ul style="list-style-type: none"> • Introduction to architecture <ul style="list-style-type: none"> ○ Hierarchy of virtual machines ○ von Neumann architecture ○ CPU instruction execution cycle ○ Overview of parallel architectures ○ I/O devices, RAID ○ Review of basic logic circuit design 	6	1,3,4
<ul style="list-style-type: none"> • Digital logic: Design of <ul style="list-style-type: none"> ○ Multiplexer, demultiplexer, encoder, decoder ○ Arithmetic Logic Unit, Shifter ○ Latch, flip-flop, register, memory organization ○ Bus protocols, arbitration, DMA ○ Data path, control unit ○ Microprogram 	14	1,3
<ul style="list-style-type: none"> • Performance enhancement <ul style="list-style-type: none"> ○ Instruction prefetch ○ Pipelining, pipeline hazards ○ Cache architecture ○ Branch prediction ○ Dynamic scheduling of instructions ○ Speculative execution 	8	2
<ul style="list-style-type: none"> • Instruction set architecture <ul style="list-style-type: none"> ○ CISC vs RISC ○ RISC Register file ○ Expanding opcode ○ Stack addressing mode ○ Flow control 	6	3,4
<ul style="list-style-type: none"> • Advanced architecture <ul style="list-style-type: none"> ○ Taxonomy of parallel architectures ○ Centralized shared memory ○ Distributed shared memory ○ Shared memory cache coherence 	5	4,5

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Course Outcomes Emphasized in Laboratory Projects / Assignments

	Outcome	Number of Weeks
1	Digital circuit design, circuit reduction Outcome: 1	3
2	Microprogram design Outcomes: 1,3	3
3	Complex microprogram design Outcomes: 1,3	3

Oral and Written Communication:

No significant coverage

Social and Ethical Implications of Computing Topics

No significant coverage

Approximate number of credit hours devoted to fundamental CS topics

Topic	Core Hours	Advanced Hours
Algorithms:		
Software Design:		
Computer Organization and Architecture:	3.0	
Data Structures:		
Concepts of Programming Languages		

Theoretical Contents

Topic	Class time
Boolean algebra	1.0

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Problem Analysis Experiences

1.

Instruction set analysis

Solution Design Experiences

1.

Digital circuit design

2.

Microprogram design

The Coverage of Knowledge Units within Computer Science Body of Knowledge¹

Knowledge Unit	Topic	Lecture Hours
AR4	Storage systems, coding, data integrity, memory organization, latency, cycle time, cache memories	6
AR5	I/O fundamentals, external storage, RAID architectures, bus protocols, bus arbitration, DMA	6
AR6	Implementation of simple datapath, control unit, pipelining, instruction level parallelism	14
AR7	SIMD, MIMD, VLIW, interconnection networks, shared memory systems, cache coherence	5
AR8	Superscalar, superpipelining, branch prediction, prefetching, speculative execution, multiple instruction issue	8

¹See <http://www.computer.org/education/cc2001/final/chapter05.htm> for a description of Computer Science Knowledge units