

## Knight Foundation School of Computing and Information Sciences

**Course Title:** Computer Architecture

**Date:** 01/15/2026

**Course Number:** CDA 3102

**Number of Credits:** 3

<b>Subject Area:</b> Computer Organization
<b>Catalog Description:</b> Covers the levels of organization in a computer: digital logic; machine and assembly language programming, design of memory, buses, ALU, CPU; virtual memory, I/O. Prerequisites: COT 3100 or MAD 2104. Corequisite: COP 3337
<b>Textbook:</b> Computer Organization and Design MIPS Edition: The Hardware/Software Interface, David A. Patterson and John L. Hennessy, 6 <sup>th</sup> Edition, Morgan Kaufmann, Dec. 2020, ISBN: 978-0128201091
<b>References:</b> Digital Design and Computer Architecture, David Money Harris and Sarah L. Harris, Morgan Kaufmann, Oct. 2021, ISBN: 978-0128200643
<b>Prerequisites Courses:</b> <a href="#">COT 3100</a> or <a href="#">MAD 2104</a>
<b>Corequisites Courses:</b> <a href="#">COP 3337</a>

Type: Required for CS Major

Prerequisites Topics:

- High level programming language constructs
- Function call/return
- Parameters of a function (method)
- Boolean algebra
- Fundamental data structures
- Number conversion among binary, octal, decimal, and hex. systems

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Course Outcomes:

1. **Explain** the instruction execution cycle of a simple von Neumann architecture by traversing the data path of various machine instructions [Understand]
2. **Develop** simple assembly language programs to perform basic computations [Apply]
3. **Apply** high-level programming constructs such as selection, iteration, and function call/return in low-level assembly representations [Apply]
4. **Describe** the purpose of interrupts and traps including their behaviors. [Understand]
5. **Design** digital logic circuits including combinational and sequential circuits [Create]
6. **Design** system components including memory and arithmetic/logic units (ALUs) [Create]
7. **Design** a control unit for a simple processor [Create]
8. **Explain** how modern processor performance is enhanced through cache organization, instruction-level parallelism mechanisms, and control-flow optimization techniques (e.g. branch prediction and multi-instruction scheduling). [Understand]
9. **Use** AI-assisted tools to deepen understanding of instruction-level behavior (e.g. exploring, translating and debugging assembly language programs). [Apply]

**Relationship between Course Outcomes and Program Outcomes**

<b>BS in CS: Program Outcomes</b>	<b>Course Outcomes</b>
a) Demonstrate proficiency in the foundation areas of Computer Science including mathematics, discrete structures, logic and the theory of algorithms	1, 5
b) Demonstrate proficiency in various areas of Computer Science including data structures and algorithms, concepts of programming languages and computer systems.	1, 2, 3, 5, 6, 7, 8
c) Demonstrate proficiency in problem solving and application of software engineering techniques	5
d) Demonstrate mastery of at least one modern programming language and proficiency in at least one other.	
e) Demonstrate understanding of the social and ethical concerns of the practicing computer scientist.	
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- f) Demonstrate the ability to work cooperatively in teams.
- g) Demonstrate effective communication skills.

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**Assessment Plan for the Course & how Data in the Course are used to assess Program Outcomes**

Student and Instructor Course Outcome Surveys are administered at the conclusion of each offering, and are evaluated as described in the School's Assessment Plan:

<https://abet.cs.fiu.edu/csassessment/>

**Outline**

Topic	Number of Lecture Hours	Outcome
<ul style="list-style-type: none"> <li>• Digital Logic &amp; CPU Building Blocks               <ul style="list-style-type: none"> <li>○ Logic gates &amp; combinational circuits</li> <li>○ Von Neumann model</li> <li>○ Instruction execution cycle</li> <li>○ Multiplexers, decoders, encoders</li> <li>○ ALU and shifter</li> <li>○ Latches, flip-flops, registers</li> <li>○ Memory organization</li> <li>○ Clocks &amp; counters</li> <li>○ Bus protocols, DMA</li> <li>○ Datapath &amp; control signals</li> <li>○ AI-assisted visualization and verification of datapath/control behavior</li> </ul> </li> </ul>	14	1, 5, 6, 7, 9
<ul style="list-style-type: none"> <li>• Assembly-level machine organization               <ul style="list-style-type: none"> <li>○ Assembly language programming</li> <li>○ Addressing modes</li> <li>○ Subroutines &amp; stack behavior</li> <li>○ System routines</li> <li>○ Interrupts &amp; traps</li> <li>○ Bit-level operations</li> <li>○ Assembly process &amp; linking</li> <li>○ AI guided code translation, debugging, &amp; register-tracking</li> </ul> </li> </ul>	14	2, 3, 4, 9
<ul style="list-style-type: none"> <li>• Performance enhancement &amp; Memory Systems               <ul style="list-style-type: none"> <li>○ Simple machine architecture</li> <li>○ Instruction prefetch</li> <li>○ Pipelining &amp; hazards</li> <li>○ Different cache architecture types</li> <li>○ Branch prediction</li> <li>○ Dynamic scheduling</li> <li>○ Speculative execution</li> <li>○ AI-assisted analysis of pipeline behavior and memory access patterns</li> </ul> </li> </ul>	9.5	8, 9

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**Tentative Weekly Schedule**

<b>Week</b>	<b>Topics</b>	<b>Course Outcome(s)</b>
1	Introduction to Computer Architecture Levels of Computer Organization Von Neumann Model	1
2	Logic Gates and Combinational Circuits Multiplexers, Decoders, Encoders	5
3	Instruction Execution Cycle Datapath Overview Control Signals	1, 7
4	ALU and Shifter Design Registers and Register Files	6
5	Sequential Logic Latches, Flip-Flops, and Registers Clocks and Counters	5
6	Memory Organization Buses, Bus Protocols, and DMA	6
7	Datapath & Control Integration AI-Assisted Visualization of Datapath Behavior	1, 7, 9
8	Assembly-Level Machine Organization Instruction Formats and Addressing Modes	2
9	Assembly Language Programming Selection and Iteration in Assembly	2, 3
10	Subroutines and Stack Behavior Function Call / Return Mechanisms	3
11	Interrupts and Traps System Routines and Bit-Level Operations	4
12	Assembly Process and Linking AI-Guided Translation and Debugging of Assembly Code	2, 3, 9
13	Processor Performance Fundamentals Pipelining and Pipeline Hazards	8
14	Cache Organization Memory Hierarchy and Cache Architectures	8
15	Advanced Performance Techniques Branch Prediction, Dynamic Scheduling, Speculative Execution AI-Assisted Analysis of Pipeline & Memory Behavior	8, 9
16	Final Exam	1-9

**Course Outcomes Emphasized in Laboratory Projects / Assignments**

	<b>Outcome</b>	<b>Number of Weeks</b>
1	Digital circuit design Outcomes: 5	2
2	Machine and assembly language programming Outcomes: 2,3	3
3	Control unit and CPU design Outcomes: 1,4,7	4
4	Memory Outcomes: 6,8	2

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5	Pipelining <p style="text-align: center;">Outcomes: 8</p>	2
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**Oral and Written Communication**

No significant coverage

<b>Written Reports</b>		<b>Oral Presentations</b>	
Number Required	Approx. Number of pages	Number Required	Approx. Time for each
0	0	0	0

**Social and Ethical Implications of Computing Topics**

No significant coverage

Topic	Class time	student performance measures

**Approximate number of credit hours devoted to fundamental CS topics**

<b>Fundamental CS Area</b>	<b>Core Hours</b>	<b>Advanced Hours</b>
<b>Algorithms:</b>		
<b>Software Design:</b>		
<b>Computer Organization and Architecture:</b>	<b>2.5</b>	
<b>Data Structures:</b>		
<b>Concepts of Programming Languages</b>	<b>0.5</b>	

**Theoretical Contents**

<b>Topic</b>	<b>Class time</b>

**Problem Analysis Experiences**

1. Instruction set analysis, Implementation of high level programming language constructs in low level languages

**Solution Design Experiences**

1. Digital circuit design
2. Assembly language programming
3. Microprogram design

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**The Coverage of Knowledge Units within Computer Science Body of Knowledge<sup>1</sup>**

<b>Knowledge Unit</b>	<b>Topic</b>	<b>Lecture Hours</b>
<a href="#"><u>PL2</u></a>	Virtual machine, hierarchy of virtual machines, intermediate languages	6
<a href="#"><u>AR1</u></a>	History of computer architecture, fundamental logic circuits, gate delays	6
<a href="#"><u>AR2</u></a>	Bits, bytes, and words, numeric data representation, fixed- and floating-point systems, signed and twos-complement representations, nonnumeric data (character codes, graphical data), representation of records and arrays	2
<a href="#"><u>AR3</u></a>	von Neumann machine, control unit; instruction fetch, decode, and execution, instruction sets and types (data manipulation, control, I/O), assembly/machine language programming, instruction formats, addressing modes, subroutine call and return mechanisms, I/O and interrupts	12
<a href="#"><u>AR4</u></a>	Storage systems, coding, data integrity, memory organization, latency, cycle time, cache memories	4
<a href="#"><u>AR5</u></a>	I/O fundamentals, external storage, RAID architectures, bus protocols, bus arbitration, DMA	2
<a href="#"><u>AR6</u></a>	Implementation of simple datapath, control unit, pipelining, instruction level parallelism	3
<a href="#"><u>AR7</u></a>	SIMD, MIMD, VLIW, interconnection networks, shared memory systems, cache coherence	2
<a href="#"><u>AR8</u></a>	Superscalar, superpipelining, branch prediction, prefetching, speculative execution, multiple instruction issue	2

<sup>1</sup>See [https://www.acm.org/binaries/content/assets/education/cs2013\\_web\\_final.pdf](https://www.acm.org/binaries/content/assets/education/cs2013_web_final.pdf) for a description of Computer Science Knowledge units

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Component	%
Exams	70
Projects	20
Homework	10

### Proposed Letter Grade Scale

Letter Grade	Percentage Range	Letter Grade	Percentage Range
A	95 or above	C+	70 – 74.99
A-	90 – 94.99	C	65 – 69.99
B+	85 – 89.99	D	60 – 64.99
B	80 – 84.99	F	59.99 or below
B-	75 – 79.99		

### Sample Assignment

#### Part 1 — Write a Short MIPS Program

Write a MIPS program that:

1. Reads an integer  $n$ .
2. Computes the sum of all even numbers from 0 to  $n$  using:
  - A loop
  - A conditional branch
  - A procedure call with stack discipline
  - A bitwise operation to test evenness

Your `compute_even_sum` procedure must return the sum in `$v0`.

#### Part 2 — AI-Assisted Review & Debugging

Using a generative AI tool of your choice:

##### A. Translation Check

- Ask the AI to explain your entire program in plain English.
- Identify two inaccuracies or omissions in the AI's interpretation and provide corrected explanations (2–4 sentences each).

##### B. Debugging Assistance

- Introduce one small bug (e.g., register misuse, wrong branch condition).
- Ask the AI to help debug it.
- Report:
  - The bug you inserted
  - The AI's suggestion
  - Whether the suggestion was correct
  - Your corrected code (3–5 lines max)

##### C. Responsible Use Reflection

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Write 5–7 sentences describing:

- How you verified AI output
- Why assembly generated by AI must be checked
- How AI helped you better understand register flow, control signals, or instruction behavior

**Part 3 — Instruction Behavior (Datapath & Control Signals)**

Select two instructions from your program (e.g., addi, and, lw, beq, jal) and for each:

1. Provide a brief datapath description (3–4 sentences) identifying source registers, ALU role, memory access (if any), and result path.
2. List the key control signals that would be active (e.g., RegDst, ALUSrc, MemRead, Branch, RegWrite, PCSrc).

(Diagrams optional but not required.)

**Submission**

Submit one PDF/DOCX containing:

- Program code
- AI explanation comparison
- Debugging documentation
- Responsible-use reflection
- Datapath + control signal analysis

**Sample Rubric (100 points total)**

1. MIPS Program Correctness — 30 pts

Grading Item	Complete (Full Credit)	Partial Credit	No Credit
<b>Program functionality</b> (even-sum logic, loop, branch, bitwise) – 12 pts	Program works correctly and meets all requirements	Minor logic or output errors	Major errors; requirements not met
<b>Procedure call &amp; stack usage</b> – 8 pts	Correct prologue/epilogue; proper use of <code>\$sp</code> , <code>\$ra</code>	Small mistakes but mostly correct	Missing or incorrect usage
<b>Code clarity &amp; comments</b> – 10 pts	Clear structure, meaningful comments	Some comments missing or unclear	Poor readability; no comments

2. AI-Assisted Analysis (CLO 9) — 30 pts

Grading Item	Complete (Full Credit)	Partial Credit	No Credit
<b>AI explanation comparison</b> – 10 pts	Identifies $\geq 2$ inaccuracies and provides correct clarifications	Identifies only one or gives limited corrections	No comparison or incorrect analysis
<b>Debugging using AI</b> – 10 pts	Bug described; AI suggestion evaluated accurately; corrected	Some details missing	No debugging analysis

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Grading Item	Complete (Full Credit)	Partial Credit	No Credit
	code provided		
<b>Responsible-use reflection</b> – 10 pts	5–7 thoughtful sentences on validation, AI limitations, and learning impact	Superficial or <5 sentences	Missing or irrelevant response

3. Instruction Behavior (Datapath & Control Signals) — 25 pts

Grading Item	Complete (Full Credit)	Partial Credit	No Credit
<b>Datapath description for two instructions</b> – 12 pts	Clear explanation of register flow, ALU role, and memory interaction	Some technical inaccuracies	Missing or incorrect
<b>Control-signal listing</b> – 8 pts	Correct key control signals for both instructions	Partially correct	Missing or wrong
<b>Instruction cycle connection</b> – 5 pts	Clear link to fetch/decode/execute behavior	Partial explanation	No explanation

4. Professionalism & Completeness — 15 pts

Grading Item	Complete (Full Credit)	Partial Credit	No Credit
<b>Organization and clarity of report</b> – 10 pts	Well-structured, readable submission	Minor formatting issues	Difficult to read or incomplete
<b>Evidence of AI interaction</b> – 5 pts	Interaction included (text or screenshots)	Partially included	No evidence provided